

**LIST OF PRIOR ART
CITED BY APPLICANT**

(Use several sheets if necessary)

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Applicant
Wadgi W. Abadeer, et al.

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PTO-1449
09/18/1995
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL*		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (if appropriate)
VN	AA	5,945,834	8/31/99	Nakata, et al.	1		
	AB	5,898,629	4/27/99	Beffa, et al.	1		
	AC	5,831,445	11/3/98	Atkins, et al.	1		
	AD	5,661,408	8/26/97	Kamieniecki, et al.	1		
	AE	5,625,297	4/29/97	Arnaudov, et al.	1		
	AF	5,600,257	2/4/97	Leas, et al.	1		
	AF	5,578,930	11/26/96	Sheen	1		
	AH	5,570,032	10/19/96	Atkins, et al.	1		
	AI	5,552,704	9/3/96	Mallory, et al.	1		
	AJ	5,528,159	6/18/96	Charlton, et al.	1		
	AK	5,519,193	5/21/96	Freiermuth, et al.	1		
	AL	5,489,974	5/12/96	Verkuil, et al.	1		
	AM	5,489,538	2/6/96	Rostoker, et al.	1		
	AN	5,485,091	1/16/96	Verkuil	1		
	AO	5,442,297	8/15/95	Verkuil	1		
	AP	5,440,241	8/8/95	King, et al.	1		
	AQ	5,412,328	5/2/95	Male, et al.	1		
	AR	5,424,651	6/13/95	Green, et al.	1		
	AS	5,399,101	3/21/95	Campbell, et al.	1		
	AT	5,429,520	7/4/93	Morlion, et al.	1		

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

VN	"WAFER LEVEL TEST AND BURN IN", IBM Technical Disclosure Bulletin, January 1992, pp. 401-404;
VN	"MULTI-LAYER CERAMIC SPACE TRANSFORMER FOR WAFER LEVEL STRESS", IBM Technical Disclosure Bulletin, April 1999, pp. 385 - 386;
VN	"WAFER BURN-IN ISOLATION CIRCUIT", IBM Technical Disclosure Bulletin, November 1989, pp. 442-443

EXAMINER *vnh Nguyen* DATE CONSIDERED 11/21/2002

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.